REMARKS

Claims 1-30 are pending in this application. Claims 1, 2, 11, 22 and 32 have been amended in several particulars for purposes of clarity and brevity that are unrelated to patentability and prior art rejections, while Claims 21-30 have been newly added in accordance with current Office policy, to alternatively define the disclosed invention over the prior art of record and expedite compact prosecution of the instant application.

The disclosure has been objected to because of the alleged improper claim of benefit under the statute. According to the Examiner, the priority benefit should have been designated under 35 U.S.C. §119 instead of 35 U.S.C. §120. Actually, the proper statutory provision is 35 U.S.C. §120 as correctly identified in the original specification since 35 U.S.C. §120, and not 35 U.S.C. §119 is the only provision that permits the Applicants to claim all benefits from a priority application that was filed in the United States. 35 U.S.C. §119 only permits the Applicants to claim benefits from a priority application that was filed in a foreign country outside the United States. In view of this explanation, Applicants trust that the objection will be withdrawn.

Claims 5-7 and 13-14 have been conditionally allowed if rewritten in independent form to include all of the limitations of their respective base claims 1 and 9. Similarly, claims 19-20 have been conditionally allowed if rewritten to overcome the rejection under 35 U.S.C. §112, second paragraph as set forth against their respective base claim 16. The Examiner's indication of allowability of these claims is noted with appreciation. For purposes of expedition, base claim 16 has been amended to overcome the rejection under 35 U.S.C. §112. Claims 21-30 have been added to alternatively define

the allowed features as defined in claims 5-7, 13-14 and 19-20. These newly formulated claims 21-30 are believed to be in condition for allowance. As for claims 5-7 and 13-14, forbearance is respectfully requested pending Applicants' traversal of the outstanding rejection of parent claims 1 and 9.

Claims 16-20 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. In particular, the Examiner asserts that base claim 16 is unclear as "there are no means for flushing and storing the table entry". Actually, the apparatus as specifically defined in the preamble of claim 16 provides the means for storing the translation and protection table (TPT) entries for virtual to physical address translations and for flushing individual translation and protection table (TPT) entry stored in accordance with a corresponding translation cacheable flag. However, in the interest of expedition, claim 16 has been amended to overcome the rejection.

More importantly, claims 16-17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Horstmann et al., U.S. Patent No. 6,125,433, as modified to incorporate selected features from Watkins, U.S. Patent No. 5,937,436. In support of this rejection, the Examiner alleges that Horstman '433, as a primary reference, teaches an apparatus which stores translation and protection table (TPT) entries for virtual to physical address translations (e.g., col. 4, lines 54-60), and which flushes individual translation and protection table (TPT) entry stored in accordance with a corresponding translation cacheable flag (i.e., valid bit) (e.g., col. 4, lines 30-34, col. 11, lines 25-35). However, the Examiner has expressly admitted that Horstmann '433 does **not** disclose the use of protection in the translation table entries. Nonetheless, the Examiner alleges that the use of protection in the translation table entries are described on col. 4, lines 41-45; col. 7, lines 55-64 of Watkins '436

which would enable one skilled in the art to make the modification in order to arrive at Applicants' claims 16-17.

This rejection is respectfully traversed, however. Applicants respectfully submit that features of the present invention are not taught or suggested by Horstmann '433 and Watkins '436, whether taken individually or in combination with any other references of record. Therefore, Applicants respectfully traverse the rejection and request the Examiner to reconsider and withdraw this rejection for the following reasons.

Independent claim 16 requires an apparatus not only to store translation and protection table (TPT) entries for virtual to physical address translations, but also to flush **individual** translation and protection table (TPT) entry stored in accordance with **a corresponding translation cacheable flag**.

In contrast to Applicants' independent claim 16, Horstmann '433 discloses the use of a cache dedicated to virtual address translations, called a translation lookaside buffer (TLB) and memory management software (MMU) used to allocate main memory to a process and store physical page number for each virtual page in the TLB in the main memory. As described on column 2, lines 66-67 of Horstmann '433, the MMU is used to flag entire unused regions and segments in the TLB as "invalid" such that the software does **not** have to mark a million translation table entries **individually** (one per page) as invalid. As shown in FIG. 5, the translation buffer (TLB) of Horstmann '433 includes a content addressable memory (CAM) column 10, a least recently used (LRU) column 11, and a random access memory (RAM) column 12. The LRU column 11 contains 64 ripple counters used to control the replacement of translation entries stored in the CAM and RAM columns.

Each row formed by the adjacent CAM, RAM and LRU columns is referred as a slice. Each slice contains a "valid bit" which indicates whether the corresponding slice contains a valid virtual to physical translation entry. At initial operations of the translation buffer (TLB), each valid bit is reset which indicates that none of the slices contain valid translation entries. When a translation entry is loaded into a slice, the valid bit included in the slice is set using the LRU algorithm to indicate that the slice contains a valid translation entry, see column 7, lines 5-30 of Horstmann '433. Therefore, the function of the valid bit as described by Horstmann '433 is to indicate whether a slice in the translation table (TLB) contains a valid translation entry.

In addition to the use of a valid bit in each slice to determine a valid translation entry, Horstmann '433 also describes the use of a "flushing" algorithm implemented within the TLB to invalidate translation entries within the TLB, see column 11, lines 25-55 of Horstmann '433. A level decoding circuit 15 as shown in FIG. 7 is used to compare the entire virtual page address with each valid entry within the TLB, and determine if a match (hit) occurs for one of the slices. If there is no match (miss), nothing is done. However, if there is a match (hit), the valid bit of that slice is reset which indicates again that the slice is able to receive another valid translation entry for replacement (even though the slice already contains a valid translation entry). According to Horstmann '433, the flushing of TLB entries is performed by the memory management software (MMU). Time can be saved since the entries do not need to be invalidated on an individual basis. When all of the TLB entries must be invalidated, each valid bit within the TLB is simply reset.

Based on the disclosure of Horstmann '433 and the explanation provided above, there is no disclosure anywhere from Horstmann '433 of Applicants' use of a corresponding translation cacheable

flag within an individual translation and protection table (TPT) entry in order to flush the individual TPT entry in accordance with the corresponding translation cacheable flag as expressly defined in claims 16-17.

Nevertheless, the Examiner cites column 4, lines 30-34, and column 11, lines 25-35 of Horstmann '433 for allegedly disclosing this feature. As discussed above, the cited portion of Horstmann '433 only refers to the valid bit used to set or reset so as to indicate if a slice contains a valid translation entry. The valid bit of Horstmann '433 is not included in each translation entry and is not used for the purpose of flushing a corresponding translation entry. In Horstmann '433, the flushing is performed by comparing the entry virtual page address with each translation entry within the TLB, and only when there is a match, resetting the valid bit to indicate that the slice is ready to receive another valid translation entry.

As a secondary reference, Watkins '436 does **not** remedy the deficiency of Horstmann '433. As correctly relied upon by the Examiner, Watkins '436 simply describes the use of protection bits 285 in a sample physical translation format 281 as shown in FIG. 2B in determining if a page is accessible using the physical translation for the virtual address as described on column 4, lines 41-45 and column 7, lines 55-64. However, Watkins '436 does **not** suggest the use of a translation cacheable flag with each TPT entry for determining whether to flush the individual TPT entry as defined in claims 16-17.

The law under 35 U.S.C. §103 is well settled that "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." *ACS Hospital System, Inc v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). The Examiner must point

to something in the prior art that suggests in some way a modification of a particular reference or a combination of references in order to arrive at Applicant's claimed invention. Absent such a showing, the Examiner has improperly used Applicant's disclosure as an instruction book on how to reconstruct to the prior art to arrive at Applicant's claimed invention.

In the present situation, Horstmann '433 and Watkins '436, whether taken individually or in combination, fail to disclose and suggest Applicants' claims 16-17. Therefore, Applicants respectfully request that the rejection of claims 16-17 be withdrawn.

Dependent claim 18 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Horstmann et al., U.S. Patent No. 6,125,433, as modified to incorporate selected features from Watkins, U.S. Patent No. 5,937,436 and Futral, U.S. Patent No. 6,112,263. In support of this rejection, the Examiner further cites Futral '263 for disclosing the use of a host comprising a host memory on column 1, lines 37-45; column 7, lines 47-55; and FIGs. 2A which enables one skilled in the art to make the appropriate modification in order to arrive at Applicants' claim 18. Applicants respectfully traverse this rejection for reasons discussed against the rejection of claims 16-17, that is, Horstmann '433 only describes the use of a valid bit to indicate if a slice contains a valid entry, and does not describe the use of a translation cacheable flag included in each TPT entry for flushing purposes.

Claims 1-4, 8-12 and 15 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Watkins, U.S. Patent No. 5,937,436, as modified to incorporate selected features from Horstmann et al., U.S. Patent No. 6,125,433, and Futral, U.S. Patent No. 6,112,263. In support of this rejection, the Examiner argues mostly that Watkins '436 does not describe the use of flushing a

translation entry in accordance with a translation cacheable flag. The Examiner also cites Horstmann '433 for disclosing this feature and Futral '263 for disclosing the use of a host including a host memory to enable one skilled in the art to make the appropriate modification to arrive at Applicants' claims 1-4, 8-12 and 15. Again, Applicants respectfully traverse the rejection also for reasons discussed against the rejection of claims 16-17 that is, Horstmann '433 only describes the use of a valid bit to indicate if a slice contains a valid entry, and does not describe the use of a translation cacheable flag included in each TPT entry for flushing purposes.

Claims 21-30 have been newly added to alternatively define Applicants' disclosed invention over the prior art of record. These claims are believed to be allowable at least for the same reasons discussed against all the outstanding rejections of the instant application.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

INTERVIEW:

In the interest of expediting prosecution of the present application, Applicants respectfully request that an Examiner interview be scheduled and conducted. In accordance with such interview request, Applicants respectfully request that the Examiner, after review of the present Amendment, contact the undersigned local Washington, D.C. area attorney at the local Washington, D.C. telephone number (703) 312-6600 for scheduling an Examiner interview, or alternatively, refrain from issuing a

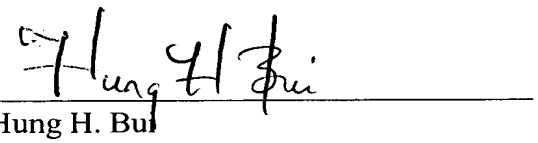
further action in the above-identified application as the undersigned attorneys will be telephoning the Examiner shortly after the filing date of this Amendment in order to schedule an Examiner interview. Applicants thank the Examiner in advance for such considerations. In the event that this Amendment, in and of itself, is sufficient to place the application in condition for allowance, no Examiner interview may be necessary.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 of Antonelli, Terry, Stout & Kraus, LLP (referencing Attorney Docket No. 219.37373X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 16-17 have been amended, and **claims 21-30** have been newly added, as follows:

16. (Amended) An apparatus, comprising:

a storage device which stores translation and protection table (TPT) entries for virtual to physical address translations, and

a mechanism which flushes individual translation and protection table (TPT) entry stored in the storage device in accordance with a corresponding translation cacheable flag included in the individual translation and protection table (TPT) entry.

17. (Amended) The apparatus as claimed in claim 16, [further comprising] wherein the storage device corresponds to an internal cache for storing said translation and protection table (TPT) entries.

21. A method, comprising:

storing, in a cache of an adapter installed in a host system and provided to interface a switched fabric, translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries

corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag; and

checking a status of the translation cacheable flag of each one or more selected TPT entries stored in the cache of the adapter to determine whether to discard one or more selected TPT entries from the cache of the adapter.

22. The method as claimed in claim 21, further comprising a step of setting the status of the translation cacheable flag per TPT entry, using an operating system (OS), for enabling the adapter to discard individual TPT entries from the cache.

23. The method as claimed in claim 21, wherein each of the TPT entries represents translation of a single page of a host memory.

24. The method as claimed in claim 21, wherein each of the TPT entries comprises:

protection attributes which control read and write access to a given memory region of the host memory;

said translation cacheable flag which specifies whether the adapter may flush a corresponding translation and protection table (TPT) entry stored in the cache;

a physical page address field which addresses a physical page frame of data entry; and

a memory protection tag which specifies whether the adapter has permission to access the host memory.

25. The method as claimed in claim 21, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether the adapter can write to a page of the host memory; a RDMA Read Enable flag which indicates whether the page can be a source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be a target of RDMA Write operation.

26. An adapter in a host system provided to interface a switched fabric, comprising:

a cache to store translation and protection table (TPT) entries from a host memory for virtual to physical address translations and access validation to the host memory during I/O transactions, each of the TPT entries corresponds to a memory portion of the host memory and comprises at least a translation cacheable flag; and

a mechanism to determine a status of the translation cacheable flag of one or more selected TPT entries stored in the cache, and to discard the one or more selected TPT entries from the cache based on the status of the translation cacheable flag.

27. The adapter as claimed in claim 26, further comprising an operating system (OS) to set the status of the translation cacheable flag per TPT entry for enabling the adapter to discard individual TPT entries from the cache.

28. The adapter as claimed in claim 26, wherein each of the TPT entries represents translation of a single page of a host memory.

29. The adapter as claimed in claim 26, wherein each of the TPT entries comprises:

protection attributes which control read and write access to a given memory region of the host memory;

said translation cacheable flag which specifies whether the adapter may flush a corresponding translation and protection table (TPT) entry stored in the cache;

a physical page address field which addresses a physical page frame of data entry; and

a memory protection tag which specifies whether the adapter has permission to access the host memory.

30. The adapter as claimed in claim 26, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether the adapter can write to a page of the host memory; a RDMA Read Enable flag which indicates whether the page can be a source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be a target of RDMA Write operation.--